L3: Entry 29 of 30 File: USPT Nov 9, 1993

DOCUMENT-IDENTIFIER: US 5260947 A
TITLE: Boundary-scan test method and apparatus for diagnosing faults in a device under test

Brief Summary Text (15):
The present invention provides a boundary-scan tester for diagnosing faults in a DUT having boundary-scan test capability. An embodiment of the invention includes a driver/receiver head for driving the input terminals of the DUT with a parallel input vector and receiving a corresponding parallel output vector from the output terminals of the DUT. Further, the tester includes means for comparing the received output vector with its expected value and providing a failure signal when the actual vector is not equal to the expected vector. A sequence controller, comparing means, receives the failure signal and in response thereto transmits control signals to the DUT via the driver/receiver head. The control signals cause actual data captured by boundary-scan cells associated with the respective input and output terminals of the DUT to be serially shifted out to the driver/receiver. A state capture RAM, coupled to the driver/receiver, stores the input/output vectors and serial boundary-scan cell data. The stored data is thereby made available for analysis to isolate the fault.

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L6: Entry 1 of 1 File: USPT May 28, 2002

DOCUMENT-IDENTIFIER: US 6397362 B1
TITLE: Fault diagnosis method and system for a sequential circuit

Detailed Description Text (101):
The present embodiment uses information of expected values for outputs of any flip-flops in the LSI obtained for all possible input vectors of the flip-flops, pass/fail information for output pins in an actual test of the LSI by a tester, and a netlist including connection information of all the nets or interconnects in the LSI, all of which are prepared beforehand. The fault diagnosis process is conducted by inference after separating the flip-flops and the combinational circuits, to obtain inferred failed paths and candidate faulty positions by coupling and connecting the inferred failed paths thus obtained for each combinational circuit. In addition, weighing of the candidate faulty positions is conducted based on the number of the failed output pins or the number of inferred failed routes carrying the failure to the failed output pins.

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L3: Entry 4 of 30 File: USPT Dec 30, 2003

DOCUMENT-IDENTIFIER: US 6671848 B1
** See image for Certificate of Correction **
TITLE: Test circuit for exposing higher order speed paths

Detailed Description Text (6):
A test program is typically used to communicate with circuit tester 10. The test program may run code that includes instructions which pre-condition device under test 20. The code may vary such device parameters as the input voltage and input clock frequency. To communicate with device under test 20, tester files commonly referred to as test patterns are used. The inputs and outputs of device under test 20 are typically stimulated and monitored using values in the test patterns. The values in the test pattern are represented by test vectors, which may direct the tester when to apply specific stimuli to a device's inputs and when to monitor a device's outputs for expected values. Therefore, the test program may run code to pre-condition device under test 20 and then call a particular test pattern. Thus, as device under test 20 is pre-conditioned, the inputs of device under test 20 may be stimulated while the outputs are monitored and compared against expected values. The test program may then provide a pass or fail indication based on the results of the comparison. As used herein, a test vector is a value or a group of values that may either be stimulus values or expected values. Test vectors may cause device under test 20 to operate in various modes. As will be described further below, a test vector may be applied to device under test 20 through hardware and as software.

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L3: Entry 28 of 30 File: USPT Apr 5, 1994

DOCUMENT-IDENTIFIER: US 5301156 A
** See image for Certificate of Correction **
TITLE: Configurable self-test for embedded RAMs

Detailed Description Text (15):
After a read operation is performed, the contents of the read register may be shifted out for comparison to an expected value in the tester. A next test vector is then shifted in and the cycle is repeated.

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